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Signature

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Applicant	:	I. Kizilyalli, et al.
Application No.	:	09/516,004
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Title	:	SELECTIVE LASER ANNEAL ON SEMICONDUCTOR MATERIAL
Grp./Div.	:	2811
Examiner	:	Ori Nadav
Docket No.	:	D8143-00330

APPELLANTS' BRIEF

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1. REAL PARTY IN INTEREST

The real party in interest is Agere Systems Guardian Corp. The rights to this application were originally assigned to Lucent Technologies, Inc., and that assignment recorded at Reel 011119/Frame 0064. The rights to this invention were transferred from Lucent Technologies, Inc., to Agere Systems Guardian Corp., pursuant to the PATENT ASSIGNMENT by and between LUCENT TECHNOLOGIES, INC. and AGERE SYSTEMS GUARDIAN CORP., dated January 30, 2001, a copy of which is attached hereto as Exhibit A.

2. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the present appeal, that are known to appellants or appellants' attorney.

3. STATUS OF CLAIMS

Claims 6-11 are pending in this application. Claims 6-11 have been rejected. The rejections of each of claims 6-11, are hereby appealed.

4. STATUS OF AMENDMENTS AFTER FINAL REJECTION

No amendments were filed after the Final Office action of December 28, 2001. A response to the Final Office action was filed on March 28, 2002 and included the appellants' arguments, but did not include claim amendments.

5. SUMMARY OF INVENTION

The present invention provides a field effect transistor gate structure formed on a surface of a semiconductor material of a first conductivity type. The field effect transistor gate includes a conductive layer and an amorphous insulative layer between the conductive layer and the surface. The amorphous insulative layer includes a dielectric constant greater than five. The present invention also provides self-aligned source and drain regions formed along the surface region, having a second conductivity type and being directly self-aligned with the gate structure. The operable field effect transistor is characterized by a gate leakage current of less than 0.1 amp per cm^{-2} during operation.

The invention is described generally in the specification from page 3, line 11 to page 13, line 17.

The invention relates to temperature-constrained processing of semiconductor materials and the semiconductor devices formed thereby. In particular, this invention relates to the localized laser annealing of semiconductor material. By locally annealing semiconductor material, the present invention provides semiconductor devices which include features in close proximity to one another, some of which are subjected to high-temperature annealing processing while others are not.

The claimed invention is therefore characterized, in one embodiment, by a gate structure that is not exposed to high-temperature annealing processes, and adjacent source and drain regions that have been annealed and activated using the localized annealing techniques of the invention.

The present invention is further characterized by the field effect transistors (FET's) including the distinguishing structural feature of self-aligned source and drain regions. This distinguishing characteristic means that the source and drain regions are automatically aligned with the edge of the transistor gate to reduce parasitic overlap capacitances. When self-aligned source and drain regions are used, they are necessarily formed after the transistor gate structure, including the gate dielectric, is formed, since the gate structure itself serves as a mask to direct the placement of the source and drain regions. Using conventional processing technologies, the source and drain regions are typically annealed after they are formed, at a high temperature of about 1000°C-1100°C to activate the dopants and achieve a desired diffusion profile.

The present invention addresses the problems which arise when the gate dielectric used in such self-aligned field-effect transistors comprises material having thermally sensitive properties. For example, Ta_2O_5 is a gate dielectric that changes from a desirable amorphous state to an undesirable polycrystalline state at temperatures in the range required for annealing the source/drain regions. In the polycrystalline state, Ta_2O_5 has a lower dielectric constant than in the amorphous form and when used as a gate dielectric results in significant leakage current from the gate structure. This leakage may be on the order of 1 amp per cm^{-2} during transistor operation. In the amorphous state, Ta_2O_5 has a dielectric constant greater than five. An advantage of the invention is that the Ta_2O_5 remains in the amorphous state as desired, suppressing leakage, while the previously formed and self-aligned adjacent source and drain areas are annealed. This is because the gate structure, including the Ta_2O_5, is not exposed to the spatially selective laser anneal.

An embodiment of the present invention is shown in Figure 1 of the present application, included in Exhibit B attached hereto, which illustrates self-aligned source/drain regions 21 and 22. According to the invention, a spatially selective anneal is effected with radiation. Source/drain regions 21 and 22 represent portions of the substrate 10 which have been implanted with a dopant impurity and require annealing. Portions 23 and 24 of substrate surface 11 overlying the intended source/drain regions 21 and 22 respectively, are selectively

irradiated to selectively heat and anneal certain exposed regions including the self-aligned source/drain regions 21 and 22. The radiation elevates the temperature of the intended source/drain regions to such temperature as will allow activation/diffusion of the implanted dopant to desired locations within the source/drain regions, and cures any defects associated with the initial implantation process. At the same time, the temperatures of other substrate regions adjoining source/drain regions 21 or 22 may become somewhat elevated due to thermal dissipation, but according to the invention, they are not elevated to peak levels or for a sufficient time duration to cause undesirable heating effects. Advantageously, because the temperature elevation is made local to self-aligned source/drain regions 21 and 22, the Ta_2O_5 dielectric layer 14 which is already in place due to the self-aligned nature of the structure, is not elevated to such temperature which causes a change from the desired amorphous state. The activation of dopants within source/drain regions 21 and 22 using this technique, provides a more controlled diffusion and conforms with temperature processing constraints. The resulting transistor with the self-aligned gate structure exhibits significantly reduced leakage current from the gate structure 13 relative to that associated with conventional high temperature processing of the source/drain diffusions. The leakage current is reduced by at least an order or magnitude, for example, from 1 amp per cm^{-2} to 0.1 amp per cm^{-2} or less. Leakage currents at or below 1 milliamp per cm^{-2} are achievable when the temperature of the Ta_2O_5 is kept below the threshold at which it would transition out of the amorphous state.

The spatially selective anneal provides a distinct temperature differential between adjacent regions on the wafer 10, such as between source/drain regions 21 and 22 and gate structure 13. Because of this advantage, the present invention allows for the FET's formed according to the invention, to include the distinguishing structural feature of self-aligned source and drain regions together with an amorphous gate dielectric. In conventional devices, such is not achievable because the gate dielectric is formed prior to the self-aligned source/drain regions and would be heated to the polycrystalline phase during the source/drain anneal.

The claimed invention offers an advantage not achievable in the art as it provides an operable field-effect transistor including an amorphous insulative gate dielectric having a dielectric constant greater than 5, and self-aligned source/drain regions. The claimed field-effect transistor is operable because it includes source and drain regions which have been annealed and activated using the localized, spatially selective annealing process which does not undesirably convert the high-k amorphous dielectric layer to a low-k polycrystalline layer.

6. ISSUES PRESENTED

The issues presented are whether the Examiner properly rejected the claims in the December 28, 2001 Office action.

The first issue presented is whether or not the Examiner properly rejected claims 6-8 under 35 USC § 112, first paragraph, as allegedly containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

The second issue presented is whether or not the Examiner properly rejected claims 6 and 7 under 35 USC § 102(e) as being allegedly anticipated by U.S. Patent No. 6,194,748 to Yu.

The third issue presented is whether or not the Examiner properly rejected claims 6-7 and 9-11 under 35 USC § 103(a) as being allegedly unpatentable over U.S. Patent No. 6,194,748 to Yu, in view of the admitted prior art or U.S. Patent No. 5,292,673, to Shinriki et al.

The fourth issue presented is whether or not the Examiner properly rejected claim 8 under 35 USC § 103(a) as being allegedly unpatentable over U.S. Patent No. 6,194,748 to Yu, the admitted prior art, and U.S. Patent No. 5,292,673 to Shinriki et al., as applied to claim 6 and further in view of U.S. Patent No. 5,596,214 to Endo.

7. GROUPING OF CLAIMS

All claims of this application do not stand and fall together. There are two independent claims in this application, claims 6 and 9. Claims 7 and 8 depend from claims 6 and claims 10 and 11 depend from claim 9. The claims can therefore be divided into two groups:

Group I: Claims 6-8 are presented as standing together;

Group II: Claims 9-11 are presented as standing together and separately from the claims of Group I.

The complete claim set is included in the Appendix (Section 9).

8. ARGUMENT

8A. Final Rejection of Claims 6-11.

In the final Office action dated December 28, 2001, claims 6-11 of the present application were rejected under 35 U.S.C. § 112, first paragraph, under 35 U.S.C. § 102(e), and also under 35 U.S.C. § 103(a).

In particular, the Examiner rejected claims 6-8 under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 6-7 were rejected under 35 U.S.C. § 102(e) as being anticipated by Yu (U.S. Patent No. 6,194,748). The Examiner further rejected claims 6-7 and 9-11 under 35 U.S.C. § 103(a) as being unpatentable over Yu (U.S. Patent No. 6,194,748) in view of admitted prior art (APA) or Shinriki et al. (U.S. Patent No. 5,292,673). Finally, the Examiner also rejected claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Yu '748, APA, and Shinriki et al. '673, as applied to claim 6, and further in view of Endo (U.S. Patent No. 5,596,214).

The final Office action of December 28, 2001 also included the Examiner's comments regarding previously filed arguments included in a Response filed by the Appellants on October 1, 2001. The October 1, 2001 Response was filed responsive to an Office action dated May 1, 2001.

On March 28, 2002, Appellants filed a Response to the final Office action of December 28, 2001. The March 28, 2002 Response did not include any claim amendments.

8B. Claims 6-8 Are Not Subject to Rejection Under 35 USC § 112, First Paragraph.

Claims 6-8 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The Examiner alleges that: "The specification recites the initial formation of self-aligned source and drain regions. The drawings illustrate that subsequent processing steps result in a final structure whose source and drain regions are not self-aligned with the gate electrode. Thus, there is no support for the operable self-aligned FET,

as recited in claim 6." The Appellants respectfully submit that these claim rejections are untenable and should be reversed, based on the reasons set forth below.

Appellants point out that the rejection by the Examiner is not substantiated by reference to specific figures. As such, Appellants' undersigned representative, Mark J. Marcelli, initiated an Examiner interview on March 5, 2002 for clarification.

In the Examiner interview of March 5, 2002, the Examiner's position appeared to be that the embodiment illustrated in Figure 5 represents subsequent processing operations performed on one of the embodiments shown in Figures 1-3 and that drain extension region 62 was somehow added to a previously illustrated embodiment to render the initially self-aligned source/drain regions now non-self-aligned. Appellants respectfully disagree with this position. Figures 1-6 are attached hereto as Exhibit B.

Claim 6 includes the feature of an **operable** self-aligned FET. The claimed "operable" FET, including the feature of self-aligned source and drain regions, is enabled by the figures in conjunction with the specification. Figures 1-3 illustrate an FET with self-aligned source and drain regions, that is, source and drain regions that are self-aligned with the gate and therefore horizontally adjacent the gate structure. The self-aligned source and drain regions may include a slight overlap region with the gate as illustrated in Figures 1-3. Figures 1-3 do not include source/drain extension regions. In conjunction with the specification, Figure 2 supports that the dopants in the self-aligned source and drain regions are activated by the annealing process illustrated in Figures 2, as required in an "operable" device. Figure 3 shows a self-aligned gate as in Figure 1, but includes a patterned reflection coating, one technique for enabling the process illustrated in Figure 2, to selectively anneal desired portions. Figure 3 is essentially the same embodiment shown in Figure 1, but with a coating formed thereover. During the annealing process, the source and drain regions remain self-aligned as shown in Figures 2 and 3. An annealed, activated source/drain area is not structurally distinguished from an unannealed source/drain region in the cross sectional structural views used, and therefore does not require separate illustration to show that the source and drain regions have been annealed and the dopants activated such that material defects in the source and drain regions are corrected. The activation by laser annealing is described in the subject specification on page 7, line 10 through page 10, line 9, in conjunction with Figures 1 and 2.

Appellants respectfully submit that the combination of figures support the claimed invention because the figures show the self-aligned source and drain region and illustrate and

describe that these regions are annealed and activated, as required in an "operable" FET device.

The term "operable," as defined in Webster's Third New Unabridged International Dictionary, is "fit, possible or desirable to use". Even though the operable FET device requires electrical connection to current/voltage sources, the FET device shown in Figure 1 or 2, is operable within the above-cited definition of the term.

It is clear that figure 5 illustrates another exemplary embodiment which differs from the exemplary self-aligned gate embodiment(s) illustrated in Figures 1-3. The exemplary embodiment in Figure 5 includes drain extension 62. Figure 5 also coincidentally illustrates another aspect of the invention as it illustrates the substrate in a phase of manufacture subsequent to that shown in Figures 1-3.

Appellants submit that it is clear to anyone of ordinary skill in the art that drain extension 62 cannot be subsequently formed onto/below the structure illustrated on Figures 1-3, and that it is inherent that Figure 5, as introduced on page 11, lines 9-15, of the subject specification, is necessarily a different embodiment than illustrated in Figures 1-3. Drain extension 62 is an exemplary additional feature which distinguishes this embodiment. This feature is absent from the embodiment(s) illustrated in Figures 1-3. Figure 5 is included to illustrate that such source and drain extension regions, too, can be annealed by the spatially selective annealing process of the present invention. Such annealing must be carried out when the drain extension 62 is exposed and therefore precludes the formation of the self-aligned source/drain structure of Figures 1-3, which is thereby a different embodiment. Just because Figure 5 also illustrates another feature - the subsequently formed vias, does not suggest that Figure 5 is a continuation of the process operations shown in Figures 1-2 or 3. Figure 5 does not suggest that the embodiment shown in Figures 1, 2 or 3, has been further processed such that initially self-aligned source and drain regions have become transformed to being non-self-aligned. Moreover, Appellants respectfully submit that it is inherent and intuitive that if source and drain regions are formed self-aligned with the gate, they remain self-aligned with the gate. The Examiner's position that the initial self-aligned regions become "un-self-aligned" due to subsequent processing steps, is untenable.

The embodiment shown in Figures 1-2, as annealed and activated, is an "operable" FET within the meaning of the defined term operable, even though illustrated without the vias shown

in Figure 5. Appellants respectfully submit that each of the embodiments are equally "operable" within the definition of the term operable because neither illustration (Figure 5 or Figure 1, for example) shows a fully completed structure with wiring and electrical connection to voltage and current sources. Yet, each is operable, within the definition of the term, as each is fit, possible or desirable to use once electrically coupled to such voltage/current sources.

As such, the "operable self-aligned FET," as recited in claim 6, is described in the specification in compliance with the requirements of 35 U.S.C. § 112, first paragraph. Claims 7 and 8 depend directly from claim 6. Therefore, the rejection of claims 6-8 under 35 U.S.C. § 112, first paragraph, should be reversed.

8C. Claims 6 and 7 Are Not Subject to Rejection Under 35 USC § 102 as Being Anticipated by Yu (U.S. Patent No. 6,194,748).

8C1. Background

In the non-final Office action dated May 1, 2001, the Examiner rejected claims 6-7 and 9-11 under 35 U.S.C. § 103(a) as being unpatentable over Yu, U.S. Patent No. 6,194,748, hereinafter Yu '748. In that Office action, the Examiner conceded on page 3, that "Yu does not teach source and drain regions being formed self-aligned with the gate structure. However, forming source and drain regions self-aligned with the gate structure are processing limitations which do not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 U.S.P.Q. 964 (Fed. Cir. 1985)." Responsive to the May 1, 2001 Office action, Appellants filed a response on October 1, 2001 and pointed out that self-aligned source and drain regions are distinguishing structural features of a semiconductor device. In support of their argument, Appellants cited a technical reference Wolf, "Silicon Processing for the VLSI Era", Vol. 2, Lattice Press, supporting that a self-aligned gate structure is a distinguishing structural feature.

In the subject final Office action of December 28, 2001, the Examiner rejected claims 6-7, this time under 35 U.S.C. § 102(e), as being anticipated by Yu '748, again alleging that self-aligned source and drain region do not carry patentable weight.

8C2. The Examiner's Contention With Regard To Claims 6 and 7.

Claims 6 and 7 include structural features that distinguish the claimed invention from Yu '748. In the Final Office action dated December 28, 2001, the Examiner rejected claims 6-7, insofar as in compliance with 35 U.S.C. § 112, under 35 U.S.C. § 102(e) as being

anticipated by Yu '748. Claim 6 is an independent claim and claim 7 depends directly from claim 6.

In the December 28, 2001 Office action, the Examiner again concedes that Yu does not teach source and drain regions being formed self-aligned with the gate structure.

The Examiner also alleges on page 3 that "forming source and drain regions self-aligned with the gate structure are processing limitations which do not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 U.S.P.Q. 964 (Fed. Cir. 1985)".

8C3. Claims 6 and 7 Recite Distinguishing Structural Features.

Appellants first respectfully point out that claim 6 does not recite a *step* of "forming source and drain regions self-aligned - - -". Rather, independent claim 6 includes the structural feature of a self-aligned source region and a self-aligned drain region. Such features are clearly structural features and are clearly and properly claimed as structural features. They are not processing limitations as suggested by the Office action nor are they claimed as process or product-by-process features.

While the Examiner cites the case of In re Thorpe, such case is not on point because the features of self-aligned source and drain regions are distinguishing physical characteristics and not product-by-process limitations, as known by one of ordinary skill in the art. In fact, no methodology for self-aligning structures is presented. Henceforth, no process limitation is claimed at all, much less a product-by-process limitation.

Moreover, Appellants respectfully submit that such features are structurally distinguished from non-self-aligned source and drain regions to warrant the reversal of the rejection for anticipation, under U.S.C. § 102(e).

Appellants first submit that one of ordinary skill in the art understands a self-aligned source/drain region to be a physical characteristic with structural advantages. Gate structures which include self-aligned source and drain regions are commonly referred to as self-aligned gate structures in the alternative.

Moreover, responsive to the Examiner's suggestion in the Interview Summary for the March 5, 2002 interview, Appellants offer the following evidence to support that 1) a self-aligned structure is structurally different from a non-self-aligned structure, and that 2) "self-aligned" structures are appropriately included as device claim features.

- In Wolf, "Silicon Processing for the VLSI Era", Vol. 2, Lattice Press, on page 318, it states: "Furthermore, the gate itself can serve as a mask during formation of the source and drain regions (by either diffusion or ion implantation)." [These are *self-aligned source and drain regions*]. "The gate thereby becomes nearly perfectly aligned over the channel, with the only overlap of the source and drain being that due to lateral diffusion of the dopant atoms. This *self-alignment* feature simplifies the fabrication sequence, increases packing density, and reduces the gate-source and gate-drain parasitic overlap capacitances."

- In Wolf, "Silicon Processing for the VLSI Era", Vol. 1, Lattice Press, on page 824, it states: "The implantation process causes the edge of these implanted ions to be automatically aligned to the edge of the gate (i.e., it is a *self-aligned* process)."

- U.S. Patent 5,185,278 to Barker, recites (in the Background Section) "Using different mask steps to form the gate electrode, and the source and drain areas often produced transistors that had a misalignment between the gate and the source and drain areas. The misalignment created variations in the gate to drain spacing between transistors which resulted in breakdown voltage variations between transistors".

- U.S. Patent 4,259,366 to Balasubramanian et al. recites "the self-aligned gate structure is defined by the first polysilicon layer deposited in a thick oxide well, followed by diffusions which cannot cross the polycrystalline silicon lines", and "the structure is a self-aligned gate structure which is performance as well as density oriented" (emphasis added).

The foregoing technical excerpts clearly provide evidence that the alignment configuration of the features is a distinct **structural feature**, not a process limitation.

- In the March 28, 2002, Response, the Appellants identified, for the Examiner's information, several U.S. patents that have issued to include self-aligned source and drain regions recited as structural features in device claims. Such patents include U.S. Patent 5,780,892 to Chen, U.S. Patent 5,434,438 to Kuo, U.S. Patent 5,418,393 to Hayden, and U.S. Patent 5,057,898 to Adan, et al.

For example, in the Adan et al., patent, claim 9 recites "The memory device of claim 1 in which the semiconductor active layer has self-aligned source and drain regions". In the Hayden patent, claim 5 recites "The thin-film transistor of claim 4, wherein the source region and the drain region are self-aligned to the gate electrode". In Chen, U.S. Patent 5,780,892, claim 4 recites "The E^2PROM cell of claim 2 further comprising: self-aligned source and drain regions disposed on . . . . .".

- Appellants further identify several other issued United States patents that include various self-aligned features recited as structural features in claims drawn to structures. Such patents include: U.S. Patent 5,308,997 to Cooper et al., U.S. Patent 6,388,298 to Gardner et al., and U.S. Patent 4,792,925 to Corda et al., for example.

Several of the above-cited references include claim language that recites a first feature being self-aligned to a further feature. For example, in Kuo, U.S. Patent 5,434,438, claim 1 recites "a second layer of polycrystalline silicon overlying the gate insulator layer and self-aligned with both the bit line terminal and the capacitor terminal". In Hayden, U.S. Patent 5,418,343, claim 5 recites Athe thin film transistor of claim 4 wherein the source region and drain region are self-aligned to the gate electrode".

The above-cited U.S. patents further support Appellants previously asserted position that various "self-aligned" features such as self-aligned source and drain regions, satisfy USPTO guidelines for structural claim features, and are not product-by-product limitations, even when drafted to actively recite that "X" feature is self-aligned to "Y" feature. Such claim language is more process-oriented than the claimed structural feature of a '"self-aligned source region" and a "self-aligned drain region".

Moreover, Appellants submit that, even when self-aligned source and drain regions are used in a process claim, they are often recited as device/structural features. For

example, claim 1 of U.S. Patent No. 4,509,991 to Taur, recites "A process for implanting self-aligned source and drain regions in a complimentary semiconductor structure . . . ."

The above-submitted evidence supports the Appellants previously asserted representation that self-aligned source and drain features are structurally distinguished features as appreciated by one of ordinary skill in the art and acceptable device claim features. These structural features provide physical advantages not achieved by non-self-aligned structures.

Since Yu does not teach or suggest self-aligned source and drain regions as conceded by the Examiner, and since such self-aligned source and drain regions are structurally significant and distinguishing device characteristics recited in claim 6, claim 6 include features that distinguish the present invention from the cited reference of Yu. Since claim 7 depends from claim 6, then, the Examiner's rejection of claim 6 and 7 under 35 U.S.C. § 102(e) as being anticipated by Yu '748, should be reversed.

8D. Claims 6-7 and 9-11 Are Not Subject to Rejection Under 35 U.S.C. § 103(a) as Being Unpatentable Over Yu (U.S. Patent no. 6,194,748) in View of Admitted Prior Art or Shinriki et al. (U.S. Patent 5,292,673).

In the Office action, specifically in paragraph 6, claims 6-7 and 9-11 were rejected under 35 USC § 103(a) as being unpatentable over Yu in view of admitted prior art (APA) or Shinriki et al. (U.S. Patent 5,292,673), hereinafter "Shinriki". Appellants respectfully submit that these rejections should be reversed based on the remarks set forth below.

It should be noted that independent claims 6 and 9 recite a combination of limitations, some of which may be separately known. It is the new combination of these limitations which is claimed and which is non-obvious under the conditions of 35 USC § 103. In fact, the claimed combination of features is mutually exclusive in conventional devices. Moreover, each of claims 6 and 9 include significant limitations other than the known limitations.

The art of field effect transistor fabrication teaches that, in order to be operable, the source and drain regions of a transistor must be annealed at an elevated temperature after the source/drain regions are formed. This annealing process utilizes an elevated temperature high enough to activate the dopant impurities, cure the defects associated with introducing impurities into a substrate, and to achieve the desired dopant profile. According to the conventional art for producing a self-aligned source and drain region, and in which the gate structure is used as a mask to form the self-aligned source and drain structures, the self-aligned source/drain regions are necessarily formed after the gate structure, including the gate dielectric and gate electrode,

is intact. This means that the annealing process necessary to achieve the desired dopant characteristics, is necessarily carried out after the gate structure including any originally high-K insulative material, is formed using conventional technology. Typical annealing processes are carried out at temperatures within the range of about 800°C-1100°C preferably 1000°C to 1100°C. Such annealing processes, necessary to produce activated source/drain regions required for a field effect transistor to be operable, will necessarily convert an amorphous insulative layer, already formed in the transistor gate in a self-designed gate structure, to a crystalline or polycrystalline structure and will therefore also lower the dielectric constant of an insulative material which may have been initially formed as a high-K dielectric material. More particularly, an originally amorphous, high-K dielectric material will necessarily be converted to a crystalline material having a dielectric constant less than five after being exposed to the elevated temperatures typically used for annealing processes. As such, according to the prior art, a self-aligned source and drain structure and an amorphous, high-K dielectric (dielectric constant >5), are mutually exclusive in an operable transistor device (i.e., one including annealed/activated source/drain regions). The advantage of the present invention is that the spatially selective annealing process allows for annealing the already formed self-aligned source and drain regions without heating the amorphous high-K dielectric material and converting it to a crystalline film having an undesirably low dielectric constant. This advantage produces the claimed structural advantages of an amorphous high-K insulative layer with a dielectric constant greater than 5 and self-aligned source and drain regions in a operable field effect transistor, as recited in amended claims 6 and 9.

The Office action states that the cited reference of Yu teaches "an amorphous tantalum pentoxide 34 layer. . . having a dielectric constant greater than 5". While Yu discloses the deposition of an originally-amorphous Ta_2O_5 layer within the gate dielectric structure, Yu does not, however, teach or suggest forming self-aligned source and drain structures in conjunction with this amorphous tantalum pentoxide layer. In fact, Yu clearly requires that the tantalum pentoxide amorphous layer and the gate itself, are formed *after* high-temperature processes (e.g., greater than 800°C) *are completed* (e.g., silicidation, dopant activation, etc.). [Yu, col. 5, ll. 53-55]. As such, according to Yu, the features of an amorphous tantalum pentoxide gate dielectric layer and self-aligned source and drain regions are mutually exclusive. Yu does not and cannot produce self-aligned source and drain regions because Yu's gates MUST be formed after the source/drain regions have been formed and annealed. While the APA and Shinriki

each disclose self-aligned source and drain regions, neither makes up for the deficiencies of Yu because neither teaches or suggests self-aligned source and drain regions in combination with an amorphous, high-K gate dielectric layer in an operable FET, i.e., an FET having source and drain regions annealed to include activated dopants as in the claimed invention.

It is the **COMBINATION** of the structural features of 1) the self-aligned source and drain regions, 2) the high-K amorphous dielectric layer having a dielectric constant greater than 5, and 3) an operable FET, such as recited in independent claims 6 and 9, that is not achievable in the prior art. It is because of various distinguishing aspects of the present invention, that the above-cited distinguishing structural features are achievable in combination.

Shinriki discloses self-aligned source and drain regions, and a tantalum oxide film included in the gate dielectric. Shinriki does not teach an amorphous insulative layer having a dielectric constant greater than 5. Furthermore, Shinriki discloses high-temperature operations necessarily carried out after the formation of the tantalum oxide film which would necessarily convert the tantalum oxide film to a crystalline structure. Shinriki discloses an 800°C oxidation process and a 900°C heat treatment following the formation of the tantalum pentoxide. Not only does Shinriki not teach or suggest the feature of an amorphous insulative layer having a dielectric constant greater than 5, the process sequence of Shinriki, in fact, renders it impossible for the tantalum pentoxide to remain a high-k amorphous dielectric layer having a dielectric constant greater than 5.

Although Shinriki, APA, and various other references teach or suggest that self-aligned source and drain features are desirable, according to the prior art, such a feature is not achievable in conjunction with the claimed features of an amorphous insulative layer having a dielectric constant greater than 5 in an operable FET transistor, as recited in claims 6 and 9. None of the cited references, taken alone or in combination, teach or suggest that COMBINATION of features as recited in claims 6 and 9. The Examiner has not upheld the responsibility under 35 USC § 103(a) to show how that of ordinary skill in the art would have been motivated to combine the reference to produce the claimed structure, because it is not possible to combine the cited references to produce the structure including the combination of claimed features.

Claim 9 includes the additional distinguishing and advantageous feature that the field effect transistor is characterized by a gate leakage current less than 0.1 amp per cm^{-2} during operation. The Examiner states that such a gate leakage current is inherent in Yu's device,

because Yu's structure is identical to the claimed structure. Appellants respectfully point out that, in the rejection under 35 U.S.C. § 102(e) of the Office action (paragraph 6) the Examiner concedes that Yu's structure differs from the claimed structure because the claimed structure includes self-aligned source and drain regions and Yu does not teach this feature. Furthermore, in the rejection under 35 U.S.C. § 103(a), the Examiner brings in two additional references to combine with Yu '748 to reject claim 9. Since Yu's structure is different from the claimed structure as conceded by the Examiner, the structural characteristic that the transistor is characterized by a gate leakage current less than 0.1 amp per cm^{-2} during operation, is not achievable in Yu '748. The cited reference of Yu '748 does not disclose or suggest gate leakage characteristics and based on the foregoing reasons, such a low leakage is not achievable using the structure provided by Yu '748. Therefore claim 9, and claims 10 and 11 which depend from claim 9, include additional features which further distinguish these claims from the references.

As such, each of independent claims 6 and 9 include features neither taught nor suggested by the cited references and are therefore distinguished from the references. Claim 7 depends from claim 6 and claims 10 and 11 depend from claim 9 and therefore the Examiner's rejection of claims 6-7 and 9-11, under 35 USC § 103(a) as being unpatentable over Yu, in view of APA or Shinriki, should be reversed.

8E. Claim 8 is Not Subject to Rejection Under 35 U.S.C. § 103(a).

In the Office action, specifically in paragraph 7, claim 8 was rejected under 35 USC § 103(a) as being unpatentable over Yu, admitted prior art and Shinriki, as applied to claim 6 above, and further in view of Endo (U.S. Patent 5,596,214), hereinafter Endo '214. This claim rejection is overcome based on the remarks set forth below.

The cited reference of Endo has apparently been relied upon for disclosing a silicon oxide layer disposed between the insulative layer and the surface region. The cited reference of Endo therefore does not make up for the above-detailed deficiencies of the references of Yu '748, APA and Shinriki '673. More particularly, Endo '214 does not enable the combination of features not achievable by Yu '748, APA and Shinriki '673. Since independent claim 6, the base claim from which dependent claim 8 depends, is distinguished from the references for reasons set forth above, dependent claim 8 is therefore also distinguished from the cited references, taken alone or in combination. Therefore, the rejection of claim 8 under 35 USC § 103(a) as

being unpatentable over Yu '748, APA and Shinriki '673, in view of Endo '214, should be reversed.

8F. Comments Regarding Examiner's Response to Arguments.

In the final Office action of December 28, 2001, specifically in paragraph 8-10, the Examiner provided commentary responsive to the arguments set forth in the Appellants' previous response of October 1, 2001.

With respect to paragraph 8 of the Office action, Appellants respectfully point out that in Yu '748, the source and drain regions are features 22 and 24, respectively, while the source extension and drain extension regions are features 23 and 25, respectively. In view of the foregoing definitions of "self-aligned regions," it is clear that the source extension and drain extension regions 23 and 25 are the structures which are directly aligned with the transistor gate, i.e., directly adjacent to gate 31 as in Figure 1 of Yu '748. Based on the foregoing definition of self-aligned, it is inherent that source and drain regions 22 and 24 and source and drain extension regions 23 and 25 cannot both be self-aligned to the gate. Therefore the source and drain regions 22 and 24 of Yu are not self-aligned to the gate as pointed out in the Appellants' argument in the October 1, 2001 Response.

In paragraph 9, the Examiner stated "Applicant did not specify which structural elements are produced as a result of the selective annealing process of the present invention which are not present in the device of Yu, APA, Shinriki et al. and Endo". As stated in paragraph 8D above, it is the **combination** of structural elements of 1) an amorphous high-k gate dielectric having a dielectric constant greater than 5, 2) self-aligned source and drain regions, and 3) an operable transistor (i.e., source/drain regions having dopants activated by annealing) that are not achievable and therefore not present in the devices of Yu '748, APA, Shinriki '673 and Endo '214. This combination of features is achievable due to the spatially selective laser anneal of the present invention. As stated in the Appellants' October 1, 2001 response and above, it is this combination of structural elements that distinguishes the present invention, and which are not present in the devices of Yu '748, APA, Shinriki '673 and Endo '214, and therefore overcomes the rejection under 35 USC § 103(a), which should be reversed as above.

8G. Conclusion.

In view of the foregoing remarks, Appellants submit that this application is in condition for allowance. Appellants respectfully request that the Board reverse the Examiner's rejection of all pending claims.

In accordance with 37 CFR §1.192(a), this Appeal Brief is being submitted in triplicate. Also enclosed is the fee for filing an Appeal Brief under 37 CFR §1.17(c) in the amount of $310.

Respectfully submitted,

DUANE MORRIS LLP

By _____
Mark J. Marcelli
Reg. No. 36,593
619/744-2243

Attachments: Appendix
Exhibits A - C

9. APPENDIX

Claims Under Appeal

6. An integrated circuit comprising:

a semiconductor material of a first conductivity type having a surface region for formation of devices;

a field effect transistor gate structure formed on the surface region, comprising a conductive layer and an amorphous insulative layer having a dielectric constant greater than five, the insulative layer formed between the conductive layer and the surface region;

a self-aligned source region formed along the surface region and having a second conductivity type; and

a self-aligned drain region formed along the surface region and having a second conductivity type, said gate structure, source region and drain region configured to form an operable self-aligned field effect transistor, said source region and said drain region directly self-aligned with the gate structure.

7. The device of claim 6 wherein the insulative layer comprises Ta_2O_5.

8. The device of claim 6 further including a layer of SiO_2 disposed between the insulative layer and the surface region.

9. A semiconductor device comprising:

a semiconductor material of a first conductivity type having a surface region for formation of devices;

a field effect transistor gate structure formed on the surface region, comprising a conductive layer and an amorphous insulative layer having a dielectric constant greater than 5, the insulative layer formed between the conductive layer and the surface region; and

a self-aligned source region and a self-aligned drain region, each formed in the surface region, directly self-aligned with the gate structure and on a different side of the gate structure,

said gate structure, source region and drain region configured to form a self-aligned field effect transistor characterized by a gate leakage current less than 0.1 amp per cm^{-2} during operation.

10. The device of claim 9 wherein the field effect transistor is characterized by a gate leakage current less than 10 milliamps per cm^{-2} during operation.

11. The device of claim 9 wherein the field effect transistor is characterized by a gate leakage current less than one milliamp per cm^{-2} during operation.

Attachments

Exhibit A. Patent Assignment between Lucent Technologies, Inc. and Agere Systems Guardian Corp.

Exhibit B. Figures 1-6 of the Application (informal drawings).

Exhibit C. References USPN 4,259,366, 4,509,991, 4,792,925, 5,057,898, 5,185,278, 5,308,997, 5,418,393, 5,434,438, 5,780,892, 6,388,298, Wolf, "Silicon Processing for the VLSI Era", Vol. 2, Lattice Press, p. 318, and Wolf, "Silicon Processing for the VLSI Era", Vol. 1, Lattice Press, p. 824.

MJM/mep

EXECUTION COPY

PATENT ASSIGNMENT

by and between

LUCENT TECHNOLOGIES INC.

and

AGERE SYSTEMS GUARDIAN CORP.

Dated as of January 30, 2001

PATENT ASSIGNMENT

THIS PATENT ASSIGNMENT (this "Assignment"), effective as of January 30, 2001 (the "Effective Date"), is by and between Lucent Technologies Inc., a Delaware corporation, with offices at 600 Mountain Avenue, Murray Hill, New Jersey 07974, United States of America, ("ASSIGNOR") and Agere Systems Guardian Corp., a Delaware corporation, with offices at 555 Union Boulevard, Allentown, PA 18109, United States of America ("Agere Systems Guardian").

RECITALS

A. WHEREAS, the Board of Directors of ASSIGNOR has determined that it is in the best interests of ASSIGNOR and its stockholders to separate ASSIGNOR's existing businesses into two independent businesses;

B. WHEREAS, ASSIGNOR presently owns or controls certain patents, patent applications, and invention submissions listed in the attached Appendices A and B (hereinafter "TRANSFERRED PATENTS") and;

C. WHEREAS, in furtherance of the foregoing separation, ASSIGNOR desires to transfer, assign, convey, deliver and vest all of its interests and rights in TRANSFERRED PATENTS for all countries, jurisdictions and political entities of the world, to and in Agere Systems Guardian;

NOW, THEREFORE, in consideration of the premises and for other good and valid consideration, the receipt and sufficiency of which are hereby acknowledged, the parties, intending to be legally bound, agree as follows:

ASSIGNOR, subject to existing rights and licenses of third parties, does hereby assign, convey, transfer and deliver, and agrees to assign, convey, transfer and deliver to Agere Systems Guardian, its successors, assigns and legal representatives or nominees, ASSIGNOR's entire right, title and interest, for all countries, jurisdictions and political entities of the world, along with the right to sue for past infringement, to all TRANSFERRED PATENTS listed on Appendices A and B, and corresponding counterpart foreign patents and patent applications, with respect to which, and to the extent to which, ASSIGNOR now has or hereafter acquires the right to so assign, convey, transfer and deliver. Agere Systems Guardian recognizes that ASSIGNOR holds only bare legal title to the TRANSFERRED PATENTS listed in Appendix A (which lists the United States Patents and patent applications previously exclusively licensed to Lucent Technologies Microelectronics Guardian Corp.).

ASSIGNOR and ASSIGNEE recognize that the patents listed in Appendices A and B may inadvertently include patents that are owned by various subsidiaries of ASSIGNOR, including Agere, Inc., Ortel Corporation, Optimay Corporation, Herrmann Technology, Inc., and Enable Semiconductor, Inc. Ownership of such patents shall not be affected by this Patent

Assignment, and ASSIGNEE agrees that any such patents shall be deemed deleted from Appendices A and B.

ASSIGNOR agrees that, upon request it will, at any time without charge to Agere Systems Guardian, but at Agere Systems Guardian's expense, furnish all necessary documentation relating to or supporting chain of title, sign all papers, take all rightful oaths, and do all acts which may be necessary, desirable or convenient for vesting title to TRANSFERRED PATENTS in Agere Systems Guardian, its successors, assigns and legal representatives or nominees; including but not limited to any acts which may be necessary, desirable or convenient for claiming said rights and for securing and maintaining patents for said inventions in any and all countries and for vesting title thereto in Agere Systems Guardian and its respective successors, assigns and legal representatives or nominees.

Execution Copy

IN WITNESS WHEREOF, the parties have caused this PATENT ASSIGNMENT to be executed by their duly authorized representatives as of the Effective Date.

LUCENT TECHNOLOGIES INC.

By: _____
Daniel P. McCurdy
President, Intellectual Property Business

AGERE SYSTEMS GUARDIAN CORP.

By: _____
Fred M. Romano
President

Execution Copy

ACKNOWLEDGMENTS

STATE OF NEW JERSEY)
: ss:
COUNTY OF SOMERSET)

I CERTIFY that on January 30, 2001, Daniel P. McCurdy personally came before me and this person acknowledged under oath, to my satisfaction that:

a.) this person signed, sealed and delivered the attached Patent Assignment as President - Intellectual Property Business of Lucent Technologies Inc.; and

b.) this Patent Assignment was signed and made by Lucent Technologies Inc. as its voluntary act and deed by virtue of authority from its Board of Directors.

Name
Notary Public
My Commission Expires:
[Notarial Seal]

TAMORA ANNE HANNA
Notary Public of New Jersey
Registered in Hunterdon County
My Commission Expires March 25, 200

STATE OF FLORIDA)
: ss:
COUNTY OF ORANGE)

I CERTIFY that on January 31, 2001, Fred M. Romano personally came before me and this person acknowledged under oath, to my satisfaction that:

a.) this person signed, sealed and delivered the attached Patent Assignment as Vice President of Agere Systems Guardian Corp. ; and

b.) this Patent Assignment was signed and made by Agere Systems Guardian Corp. as its voluntary act and deed by virtue of authority from its Board of Directors.

Name
Notary Public
My Commission Expires:
[Notarial Seal]

MARY V CARTER
MY COMMISSION # CC 969433
EXPIRES: Sep 20, 2004
1-800-3-NOTARY FL Notary Service & Bonding, Inc.

APPENDIX B (continued)
Transferred Patents

Case Name	Filing Date	Issue Date	Patent No.	Serial No.
Kizilyalli 39-36-72-80	6/25/1999			09/339895
Kizilyalli 41-5	6/25/1999			09/339894
Kizilyalli 42-77-17	6/3/1999			09/325624
Kizilyalli 43-78-18	11/17/1999			09/441561
Kizilyalli 45-97-112	7/27/1999			09/361733
Kizilyalli 46-19-123	2/29/2000			09/516004
Kizilyalli 49-20-1	5/17/2000			09/572060
Kizilyalli 53-6-12	8/28/2000		09/648997	
Kizilyalli 6-2	3/22/1996		08/621047	
Kizilyalli 8-8-32	12/22/1997		08/995589	
Kizilyalli 9-9-33	12/22/1997		08/995435	
Knaeblein 1-1	6/11/1999			09/330862
Knoedl 20	5/27/1999			09/321004
Knoedl 21	3/5/1999			09/263445
Knoedl 22	1/5/2000			09/475575
Knolle 2-2	10/19/1987		07/110153	
Koc 1-2-5-1-1	7/2/1999			60/142100
Koenig 1-6	6/30/2000			09/607337
Kohler 4	6/23/1998		09/103095	
Kohler 5-9	5/19/1999			09/314741
Kola 12-16-12	4/14/1999			09/291781
Kolagotla 14-9	8/27/1997	4/11/2000	6049858	
Kolagotla 16-10	8/27/1998		09/140959	
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Kolsrud 5	8/27/1998		09/141569	
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Kopylov 7-11	8/25/1999			09/382611
Komblit 13-7-19	7/23/1998	4/18/2000	6051346	
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Kossives 21-23-16-24-40	1/18/2000			09/484498
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Kothandaraman 2-20-4-3	4/28/1998	5/16/2000	6064231	
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Krutsick 3	4/18/2000			09/551050
Krutsick 4	8/30/2000		09/650808	
Krutsick 5	8/30/2000		09/650604	
Kuehne 2-13	7/10/1998		09/113583	
Kuehne 5-33-10	6/26/2000			09/603340
Kuhn 2-6-1	8/3/2000		09/631862	
Kurshan 25-1	7/2/1999			09/347628
Kwong 2	8/19/1999			09/377851
Lai 11	6/10/1999			09/329465
Lai 14-3	9/9/1999			09/392380

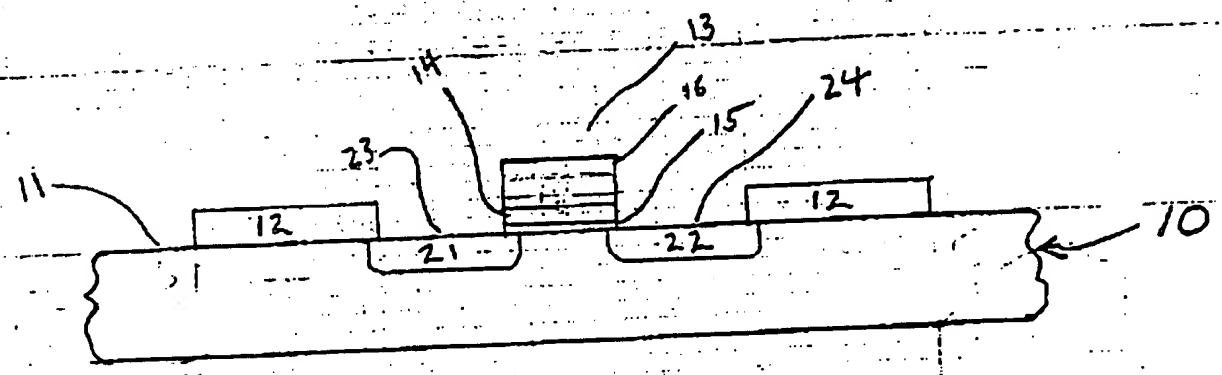

Figure 1

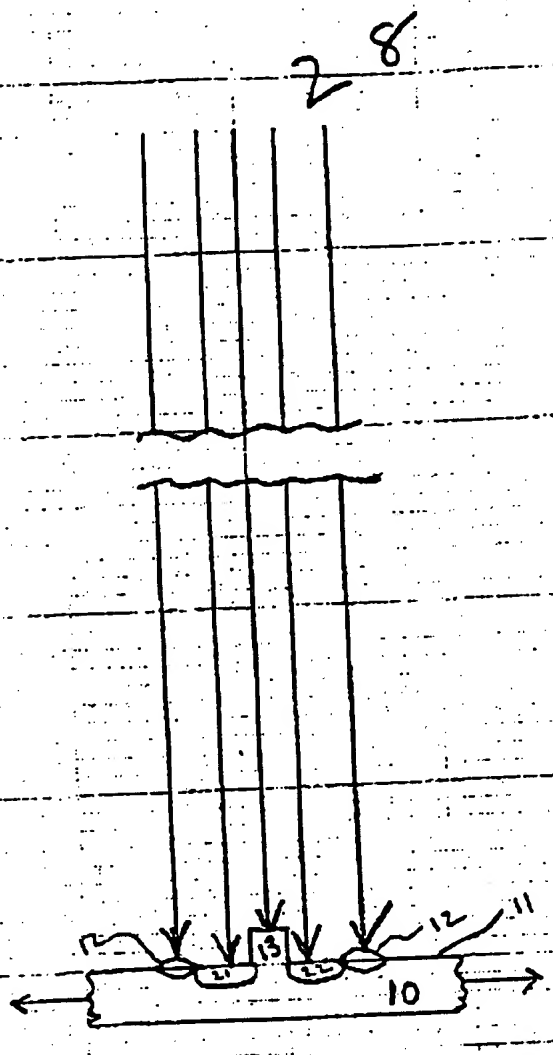

Figure 2

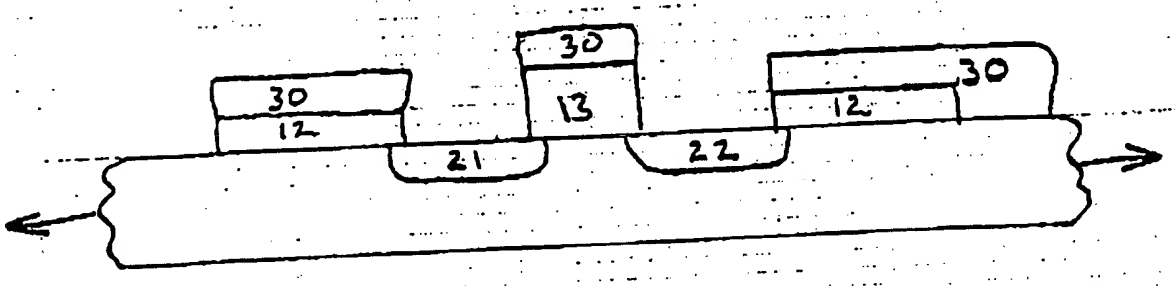

Figure 3

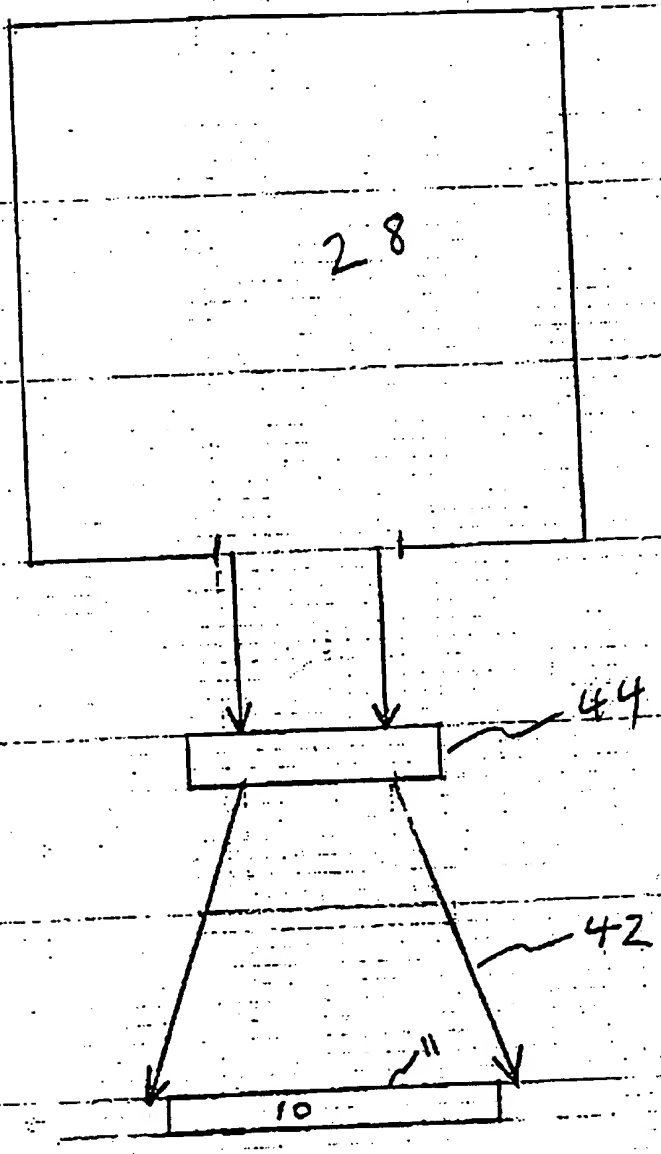

Figure 4

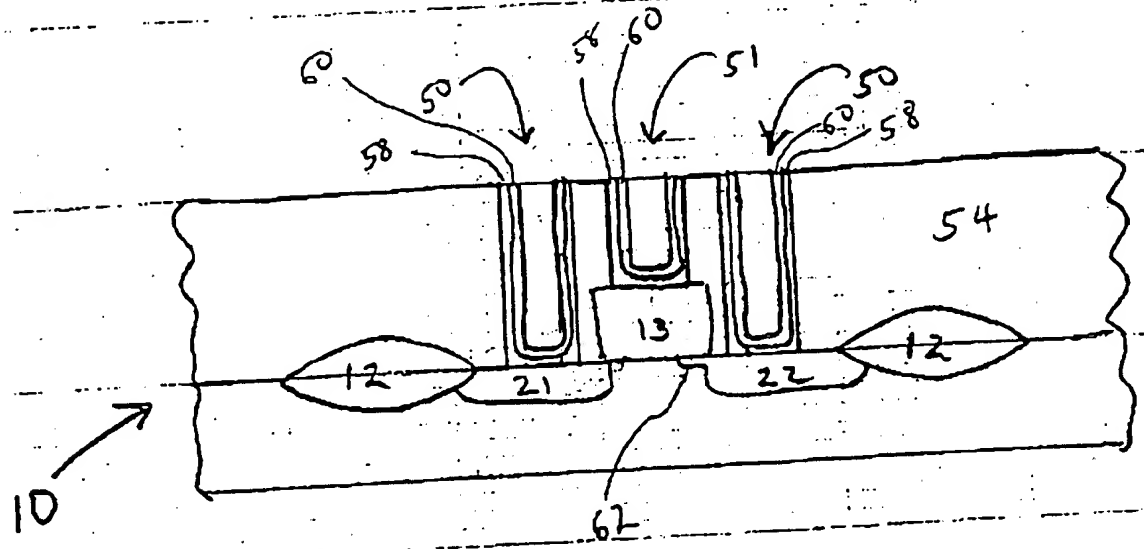

Figure 5

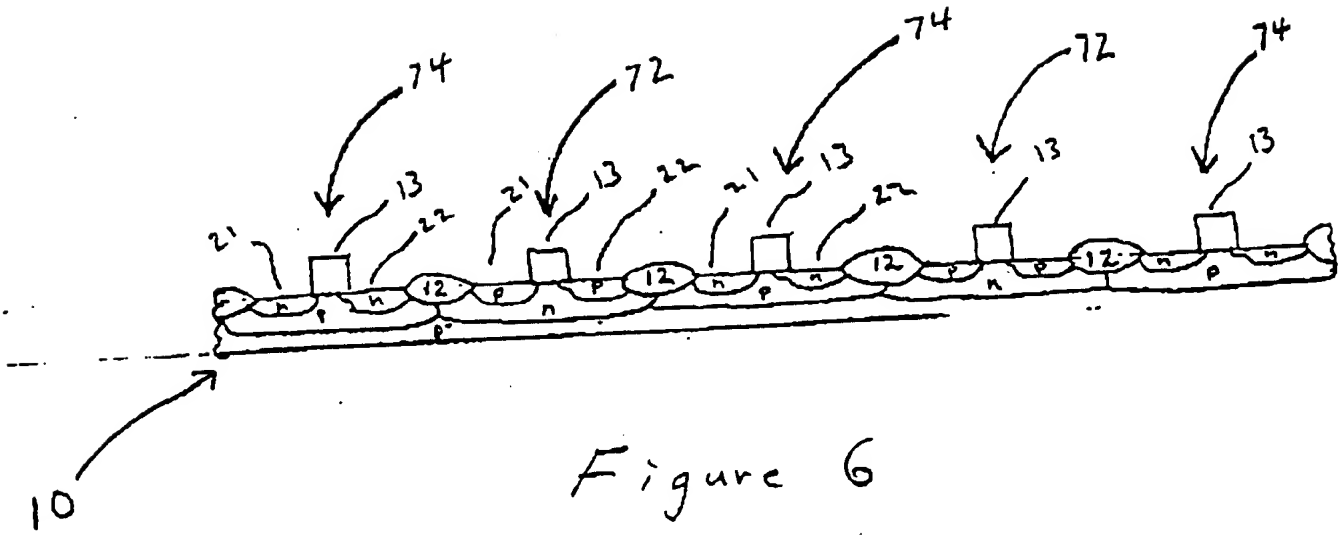

Figure 6

SILICON PROCESSING

FOR

THE VLSI ERA

VOLUME 2:

PROCESS INTEGRATION

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LATTICE PRESS

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5.3.2 Silicon-Gate MOS Technology

One of the key process innovations for MOS ICs was the use of heavily doped polysilicon as the gate electrode in place of Al (see Vol. 1, chap. 6 for more information on polysilicon thin films). The development of this *silicon gate technology* improved the fabrication of MOS ICs in the following ways:

- Since aluminum must be deposited following completion of all high-temperature process steps (including drive-in of the source and drain regions), the gate electrode must be separately aligned to the source and drain. This alignment procedure adversely affects both packing density and parasitic overlap capacitances between the gate and source/drain regions. Since polysilicon has the same high melting point as the silicon substrate, it can be deposited prior to source and drain formation. Furthermore, the gate itself can serve as a mask during formation of the source and drain regions (by either diffusion or ion implantation). The gate thereby becomes nearly perfectly aligned over the channel, with the only overlap of the source and drain being that due to lateral diffusion of the dopant atoms. This *self-alignment* feature simplifies the fabrication sequence, increases packing density, and reduces the gate-source and gate-drain parasitic overlap capacitances.

- The threshold voltage of PMOS devices is reduced by the use of a polysilicon gate, since the φ_{ms} is less negative (see Eqs. 5-2). For PMOS devices on <111>- Si, the threshold voltage is reduced from roughly -4 V to -2 V. This smaller threshold voltage value enabled PMOS ICs to become compatible with TTL (bipolar) ICs, allowing MOS to be designed into many digital systems that operated at TTL-defined power supply voltage levels (i.e., 0 V to 5 V).

- The ability of polysilicon to withstand high temperatures also permits it to be completely encapsulated by an SiO_2 layer. This allows the polysilicon film to function as an interconnect path, in addition to serving as the gate electrode. By taking advantage of this new interconnection structure (without having to use a second layer of metal, as was necessary with bipolar ICs), it was possible to give MOS ICs an additional level of interconnection that could be crossed by the usual metal layer, or even by another polysilicon layer. This eased the problem of routing the electrical paths among the devices of an IC, thereby facilitating the layout of compact digital integrated circuits. (Techniques for establishing contact between the polysilicon layer and substrate are described in chap. 3, section 3.11.1). The ability of polysilicon to withstand high temperatures was also exploited to allow the dielectric (e.g. phosphorus-doped SiO_2) that covers it to be flowed, thereby making a significantly smoother surface topography for metallization layers.

The greatest disadvantage of polysilicon as a gate material compared to Al is its significantly higher resistivity. Even when doped at the highest practical

SILICON PROCESSING FOR THE VLSI ERA

VOLUME 1:

PROCESS TECHNOLOGY

Second Edition

STANLEY WOLF Ph.D.

RICHARD N. TAUBER Ph.D.

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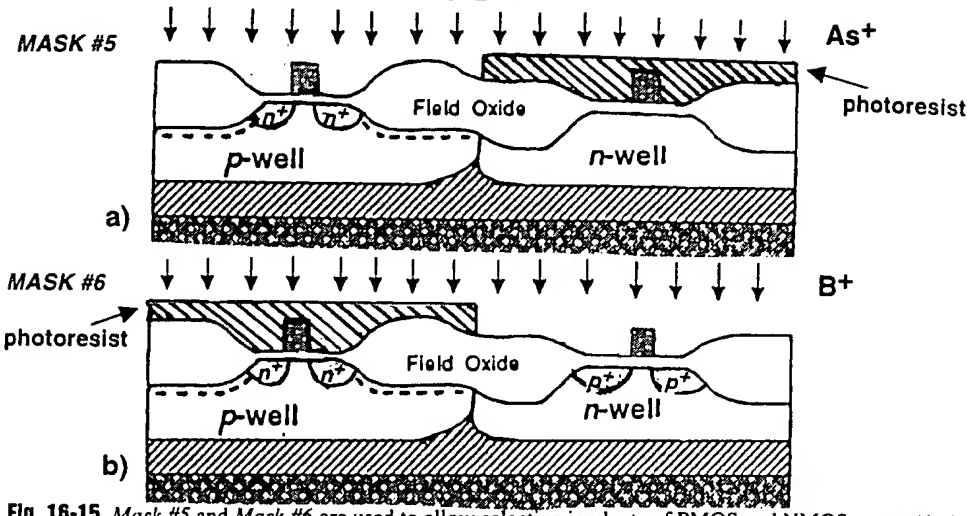

Fig. 16-15 *Mask #5* and *Mask #6* are used to allow selective implants of PMOS and NMOS source/drains.

The LDD structure is formed in the following way. The lightly doped regions of the source and drain are created with an ion implant step (Fig. 16-16b). A dose of approximately $3x10^{13}$–$3x10^{14}$ cm^{-2} dopant ions is implanted at low energy (30–50 keV). The implantation process causes the edge of these implanted ions to be automatically aligned to the edge of the gate (i.e., it is a *self-aligned process*). A conformal layer of dielectric material (usually SiO_2 or silicon nitride) is then deposited over the entire wafer. An anisotropic etch process is used to clear the oxide in the flat areas while leaving sidewall spacers on the sidewalls of the poly gates (Fig. 16-16c). These spacers cover and protect the regions beneath them from the subsequent high-dose implant that forms the rest of the S/D regions. A dose of $1x10^{15}$–$5x10^{15}$ atoms/cm^2 at 40–80 keV is used for this step (as shown in Fig. 16-16d).

16.2.8 Premetal Oxide Deposition and Contact Formation: Following formation of the source and drain regions, a doped *premetal dielectric* (*PMD*) is deposited by CVD. (This layer is also known as an *interlevel dielectric* or *ILD*.) Contact windows are opened in this dielectric layer to allow electrical connections to be made between Metal 1 and the following structures: 1) source/drain contact regions: 2) gate contacts; 3) substrate-contact regions; and 4) well-contact regions. A CVD process is used to deposit doped SiO_2, about 1 μm thick (Fig. 16-17a), onto the wafers (see Chap. 6 for details of this process). The dopant in the SiO_2 is either phosphorus (in which case the material is referred to as *phosphosilicate glass* or *PSG*), or both phosphorus and boron (making it *borophosphosilicate glass* or *BPSG*).

The doped CVD glass layer plays several roles in the fabrication and operating aspects of the circuit. First, it acts as an insulating layer between polysilicon and Metal 1. Second, it reduces the parasitic capacitance between Metal 1 and the substrate. Third, the addition of phosphorus to the glass makes the layer an excellent getter of Na ions (contamination by Na can destabilize the V_T of an MOS device). The PSG (or BPSG) binds otherwise mobile Na atoms within the doped-glass layer, preventing them from reaching the gate oxide and altering V_T. Finally, the dopants in the glass make it viscous at elevated temperatures (1000–1100°C for PSG, 850–950°C for BPSG, see Ch. 6). This allows the layer of glass to be flowed after it is deposited (Fig. 16-17b).